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10/763,304	01/23/2004	Shajan Mathew	IME03-011	6523

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EXAMINER	
DANG, TRUNG Q	
ART UNIT	PAPER NUMBER
2823	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,304	MATHEW ET AL.	
	Examiner	Art Unit	
	Trung Dang	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-28 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14-28, and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 9-12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai et al. in view of Deshpande et al., all of record.

The rejection is maintained as of record and repeated herein.

With reference to Figs 2A-2C, Bai teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate dielectric layer **202** on said semiconductor substrate (Fig. 2A);

forming a conductive layer **206** (TiN or TaN) on said gate insulator layer (col. 4, lines 18-19), wherein said conductive layer is formed of a single material *(note that the TiN or TaN is considered as a single material for the reason set forth in the previous Office action dated 9/6/06. That is, the claimed limitation "single material" does not necessarily mean a single metallic element, hence the TiN or TaN is considered as a single material consisting of two elements)*;

forming an amorphous silicon (a-Si) layer **208** (about 500 Å), wherein said amorphous silicon layer is formed of a single material, **directly** on said conductive layer **206** (col. 4, lines 33-55);

(note that the a-Si layer 208 is formed immediately after formation of the underlying conductive layer 206, thus precluding the formation of any intervening material. Accordingly, newly added limitation "without inclusion of any interceding steps immediately..." is anticipated by the reference)

defining a conductive gate structure and an overlying a-Si shape, on said gate insulator layer (Fig. 2B and col.4, lines 58-64);

removing portion of said gate insulator layer not covered by said conductive gate structure (Fig. 2B);

forming a first doped region **214** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. B and col. 5, lines 1-5);

forming nitride spacers **212** on the sides of said conductive gate structure and on the sides of said a-Si shape (Fig. 2B and col. 5, lines 6-11);

forming a second doped region **216** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said nitride spacers (Fig. 2B and col. 5, lines 11-15);

forming a metal layer **218,** wherein said metal layer is formed of a single material such as Ti, Co, Pd, Pt, or Ni by sputtering (physical vapor deposition) (Fig. 2B and col. 5, lines 33-60) ;

performing a rapid thermal annealing (RTA) procedure to form first metal silicide regions from an overlying first portion of said metal layer and from a top portion of said second doped region **216**, and to form a second metal silicide region **220** directly on said conductive gate structure from an overlying second portion of said metal layer via total consumption of said a-Si shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers (Fig. 2C and col. 6, lines 1-58).

Also, see col. 4, lines 38-39 for the teaching that the a-Si layer **208** is completely consumed during the silicide reaction.

Bai differs from the claims in not disclosing that the nitride spacers **212** are formed of a composite material comprises an oxide liner and a nitride layer. Deshpande teaches a composite insulator spacer comprises an oxide liner 22 and a nitride layer 24, wherein the oxide liner 22 having a thickness of 2 - 400 Å (col. 5, lines 62-65) and the nitride layer 24 having a thickness of 20 - 1,000 Å (col. 6, lines 9-32). It would have been obvious to one for ordinary skill in the art to form the nitride spacer **212** consisting of an oxide liner and a nitride layer having thicknesses as suggested by

Deshpande because the oxide liner acts as a buffer to reduce stress generated by the overlying nitride layer and therefore improves insulation between the gate electrode and source/drain regions.

For claims 2-4, see col. 5, lines 25-26.

As for claims 5 and 6, Bai differs from the claims in not disclosing that a high dielectric constant (high-k) material is used for the gate dielectric layer **202.** Deshpande teaches a gate dielectric layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). The subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Bai's teaching by forming the gate dielectric layer **202** using the high-k dielectrics because the selection of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art.

For claim 9, see col. 4, line 62-64 in Bai.

For claim 10, see the thicknesses of the oxide liner 22 and the nitride layer 24 mentioned above.

For claim 11, see Bai col. 5, lines 42-60 for the thickness of the metal layer 218.

For claim 12, see Bai col. 6, lines 5-15.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Despande as applied to claims 1-6, 9-12 and 14 above, and further in view of Wu

(US 6,130,135 of record).

The rejection is maintained as of record and repeated herein.

The combined process of Bai and Deshpande teaches a method as noted above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Deshpande as applied to claims 1-6, 9-12 and 14 above, and further in view of Tsai et al. (US 2002/0192932 of record) and Wieczorek et al. (US 6,274,511 of record).

The rejection is maintained as of record and repeated herein.

The combined process of Bai and Deshpande teaches a method as noted above. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH – H_2SO_4 as claimed. Wieczorek teaches that unreacted refractory metal is removed using typical solution such as HCl:H_2O_2 and H_2SO_4:H_2O_2 (col. 6, lines 37-43; hereinafter solution A). Tsai teaches unreacted refractory metal is removed

using a solution such as $NH_4OH:H_2O_2$ (para. [0026]; hereinafter solution B). Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process of Bai and Deshpande using a mixture comprises $HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

5. Claims 16-21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Despande as applied to claims 1-6, 9-12 and 14 above, and further in view of Wieczorek et al. cited above.

The rejection is maintained as of record and repeated herein.

The combined process of Bai and Deshpande teaches a method as noted above, including the first RTA step to form the silicide layers **220**. Note that since claim 16 employs "comprising" format, the claimed limitation " a metal gate structure and an overlying amorphous silicon shape" recited in claim 16 does not necessarily limit to a gate structure consisting of a metal layer and an overlying amorphous silicon layer, hence Bai's gate structure consists of a composite **metal layer 206/polysi 204** and an overlying amorphous silicon shape **208** reads on the aforementioned limitation.

The combination differs from the claims in the step of performing a second anneal procedure.

Wieczorek teaches that after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Bai and Wieczorek by performing a second annealing step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claims 25 and 26, see Deshpande, col. 5, line 51 and col. 6, line 17 for the teaching that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art. It is noted that applicants did not challenge the Examiner's Official notice in response to the previous Office action.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Despande and Wieczorek as applied to claims 16-21 and 24-28 above, and further in view of Wu cited above.

The rejection is maintained as of record and repeated herein.

The combined process of Bai taken with Deshpande and Wieczorek teaches a

method as noted above. The combination differs from the claim in not disclosing that the a-Si layer **208** is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer **208** by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

7. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bai taken with Deshpande and Wieczorek as applied to claims 16-21 and 24-28 above, and further in view of Tsai cited above.

The rejection is maintained as of record and repeated herein.

The combined process of Bai taken with Deshpande and Wieczorek teaches a method as noted above, including the teaching of using the aforementioned solution A to remove unreacted refractory metal. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of HCl - H_2O_2 - NH_4OH - H_2SO_4. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above.

Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the

combined process using a mixture comprises $HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

8. Claims 1-4, 6-7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau et al. (US 5,625,217 of record) in view of Nguyen et al. (US 6,084,279 of record).

The rejection is maintained as of record and repeated herein.

With reference to Figs 4A-4G, Chau teaches a method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer **502** (20-200 Å) on said semiconductor substrate (col. 4, line 9);

forming a conductive layer **504** of *a single material* including sputtered TiN, W, and Co having thickness 20-2,000 Å on said gate insulator layer (col. 2, line 13; col. 4, lines 14-45);

forming a polysilicon layer **506** (3,500 Å) directly on said conductive layer (col. 4, lines 53-60);

(note that the polysilicon layer 506 is formed immediately after formation of the underlying conductive layer 504, thus precluding the formation of any intervening material. Accordingly, newly added limitation "without inclusion of any interceding steps immediately..." is met by the reference except that layer 506 is of polysilicon instead of amorphous silicon as claimed)

defining a conductive gate structure and an overlying polysilicon shape, on said gate insulator layer (Fig. 4B);

removing portion of said gate insulator layer not covered by said conductive gate structure (col. 6, lines 16-17);

forming a first doped region **514a/514b** in an area of said semiconductor substrate not covered by said conductive gate structure (Fig. 4C and col. 5, lines 27-30);

forming composite insulator spacers on the sides of said conductive gate structure and on the sides of said semiconductor shape (col. 5, lines 43-53);

forming a second doped region **520a/520b** in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers (Fig. 4E and col. 6, lines 1-3);

forming a metal layer **522** of *a single material* including Ti and W (Fig. 4F and col. 6, lines 22-24) ;

performing an anneal procedure to form first metal silicide regions **524** from an overlying first portion of said metal layer and from a top portion of said second doped region, and to form a second metal silicide region on said conductive gate structure from an overlying second portion of said metal layer and from a portion of said polysilicon shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers (Fig. 4G and col. 6, lines18-35).

Chau differs from the claims in not disclosing that a) the semiconductor layer **506** is of amorphous silicon and b) the metal silicide **524** is formed via total consumption of said amorphous silicon shape.

For issue a), Nguyen teaches a metal gate structure in which amorphous silicon **68** or polysilicon can be used for the gate structure. The amorphous silicon is doped either insitu (i.e., during deposition) or during separate doping step (col. 5, lines 25-27).

It would have been obvious to one of ordinary skill in the art to modify Chau's teaching by replacing the polysilicon layer **506** with amorphous silicon because the substitution of art recognized equivalents as shown by Nguyen would have been within the level of one skilled in the art, and the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination (MPEP 2144.07).

For issue b), Nguyen teaches a method for making a metal gate structure in which silicide **85** is formed via total consumption of amorphous silicon gate structure **68** (Figs. 7-8 and col. 5, lines 65-66).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Chau's teaching by forming silicide **524** via total consumption of the amorphous silicon gate **512** as suggested by Nguyen because converting totally the gate electrode **512** to metal silicide would reduce the gate resistance and hence improve the performance of the device

For the limitation of claim 4, see col. 4, lines 20-22 and col. 6, lines 50-57.

9. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen as applied to claims 1-4, 6-7, and 9 above, and further in view of Deshpande cited above.

The rejection is maintained as of record and repeated herein.

The combined process Chau and Nguyen teaches a process for forming a MOSFET device as noted above. The combination differs from the claims in not disclosing a) a high dielectric constant (high-k) material is used for the gate dielectric layer **502** and b) the thickness of the nitride spacer **518a/518b**.

Deshpande teaches a gate dielectric layer could be a conventional dielectric material such as SiO_2, or alternatively, high-k dielectrics such as oxides of Ta, Zr, Al (col. 4, lines 20-25). Furthermore, Deshpande teaches the thickness of a nitride spacer

of a MOSFET device having LDD regions is typically from about 20 Å to about 1,000 Å (col. 6, lines 9-32).

As for issue a), the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined process by forming the gate dielectric layer **502** using the high-k dielectrics because the substitution of art recognized alternatives as shown by Deshpande would have been within the level of one skilled in the art, and the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination (MPEP 2144.07).

As for issue b), it would have been obvious to one for ordinary skill in the art to form the nitride spacer in Chau having a thickness suggested by Deshpande because such thickness for a nitride spacer is typical in the art, and utilizing a known value to made the same would have been within the level of one skilled in the art.

10. Claims 16-22, 24-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen and Deshpande as applied to claims 5 and 10 above, and further in view of Wieczorek cited above.

The rejection is maintained as of record and repeated herein.

The combination of Chau, Nguyen and Deshpande teaches a method as described above. The combined process differs from the claims in that the combined process performs the annealing once instead of twice as claimed.

Wieczorek teaches after a first RTA to form silicide, a second anneal procedure is performed to lower the resistivity of the silicide layer (col. 6, lines 44-46). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching of Chau, Nguyen and Deshpande by performing a first anneal step using RTA to form metal silicide and then performing a second RTA step after the first RTA step for the benefit of reducing the resistivity of the silicide layer as suggested by Wieczorek.

For claims 25 and 26, see Deshpande, col. 5, line 51 and col. 6, line 17 for the teaching that the oxide liner and the nitride spacer are both formed by plasma-assisted CVD (corresponding to the claimed PECVD). As for the limitation regarding the LPCVD, the examiner takes official notice that deposition of silicon oxide and silicon nitride by means of LPCVD is well known in the art. It is noted that applicants did not challenge the Examiner's Official notice in response to the previous Office action.

For claim 28, see Wieczorek, col. 6, lines 10-15 for the parameters of the first RTA.

11. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen, Deshpande and Wieczorek as applied to claims 16-22, 24-26 and 28 above, and further in view of Wu cited above.

The rejection is maintained as of record and repeated herein.

The combination teaches a process as described above. The combined process differs from the claim in not disclosing that the a-Si layer is deposited by LPCVD or PECVD. Wu teaches that a-Si can be deposited by means of LPCVD or PECVD (col. 3, lines 6-9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined teaching by depositing the a-Si layer by means of LPCVD or PECVD as suggested by Wu because such technique is known in the art, and the employment of an old process to make the same would have been within the level of one skilled in the art.

12. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chau taken with Nguyen, Deshpande and Wieczorek as applied to claims 16-22, 24-26 and 28 above, and further in view of Tsai cited above.

The rejection is maintained as of record and repeated herein.

The combination teaches a method as described above, including the teaching of using the aforementioned solution A (see Wieczorek) to remove unreacted refractory metal. The combination differs from the claim in not disclosing that the unreacted refractory metal portions are removed via a wet etching using a solution comprises of $HCl - H_2O_2 - NH_4OH - H_2SO_4$. Tsai teaches unreacted refractory metal is removed using a solution B as mentioned above. Absent a showing of new or unobvious results, it would have been obvious to one of ordinary skill in the art to remove the unreacted refractory metal in the combined process using a mixture comprises

$HCl:H_2SO_4:NH_4OH:H_2O_2$ as suggested by Wieczorek and Tsai because each member (i.e., solution A and solution B) of the mixture is known individually to wet etch the refractory metal, therefore one of ordinary skill in the art would reasonable expect such mixture to etch the refractory metal in an additive or cumulative manner.

Response to Arguments

13. Applicant's arguments filed 12/11/06 have been fully considered but they are not persuasive.

With respect to Bai's reference, applicants in page 12 of the Remarks argue that "independent claims 1 and 16 now describe an amorphous silicon layer formed immediately after formation of the underlying first metal or first conductive layer, thus precluding the use or fromation of any intervening material such as layer 206 in the Bai et al prior art." The Examiner disagrees. As noted in the rejection, it is the TiN or TaN layer 206 that reads on the claimed conductive, not conductive layer 204. Immediately after forming the conductive layer 206, the amorphous silicon layer 208 is formed directly on said conductive layer 206 as shown in Fig. 2A and related text. Thus, the claimed limitation "without inclusion of any interceding steps immediately forming an amorphous silicon layer, wherein said amorphous silicon layer is formed of a single material, directly on said conductive layer" of independent claim 1 is met by the reference. As for the Examiner's statement in the Office action dated 09/06/2006 as mentioned by applicant, the record shows the Examiner addressed his position that

"since claim 16 employs comprising format, which does not exclude other intervening steps, the claimed limitation" a metal gate structure and an overlying amorphous silicon shape" recited in claim 16 does not necessarily limit to a gate structure consisting of a metal layer and an overlying amorphous silicon layer, hence Bai's gate structure consists of a composite metal layer 206/polysi 204 and an overlying amorphous silicon shape 208 reads on the aforementioned limitation." This has nothing to do with the rejection of claim 1. As for the rejection of claim 16, because the composite metal layer 206/polysi 204 is considered to read on the claimed first metal layer for the reason set forth above, formation of the a-Si layer 208 immediately after the formation of the composite metal layer is without performing any interceding steps as claimed.

As for Chau's reference, applicants argue that "No combination of the above prior art describe **an amorphous silicon shape, (formed of a single material) and formed directly on the underlying conductive shape, (also formed of a single material) which in turn directly overlays a gate insulator layer, wherein an amorphous silicon layer used to form the amorphous silicon shape is immediately formed (without any interceding steps) on an underlying material and where the amorphous silicon shape is totally consumed during salicide formation.** It is obvious the Chau prior art does not totally consume the amorphous silicon layer overlying a conductive layer, therefore only forming metal silicide on an unconsumed portion of the amorphous silicon layer."

The Examiner respectfully disagrees. Chau's reference was employed in the rejection to show all features of the claims except for the semiconductor layer **506** is of amorphous silicon and the metal silicide **524** is formed via total consumption of said amorphous silicon shape. It is the Nguyen reference that cures the deficiency in Chau, i.e., Nguyen provides logical reasons as to why one of ordinary skill in the art would motivate to make the combination as addressed in the rejection. Applicants are reminded that it is axiomatic that one cannot show nonobviousness by attacking references individually where the rejection, as here, is based on a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). For example, applicants argue that Chau does not teach or suggest the claimed feature as mentioned above. However, the combined process of Chau and Nguyen, not Chau nor Nguyen alone, is employed in the rejection to show an amorphous silicon layer is formed directly on the conductive layer 504 of a single material such as TiN, W, or Co, and said amorphous silicon layer is totally consumed by the subsequent silicidation process. That is, Chau's reference is relied in the rejection to show the **immediate** formation of the polysilicon layer 506 directly on the conductive layer 504 and therefore **without any interceding steps**, which in turn directly overlays gate insulator 502. On the other hand, Nguyen' s reference, not Chau, is relied in the rejection to provide logical reason as to why one skilled in the art would motivate to replace the polysilicon layer 506 with an art-recognized equivalent material such as amorphous silicon, and thereafter total

consumption of said amorphous layer in the silicidation process. Thus, the claims are met by the combined teachings of the references, not by a single reference as alleged by applicants.

For claim 16, again, the claim is met by the combined teachings of the references as clearly addressed in the rejection, not by a single reference as alleged by applicants.

Conclusion

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang

Trung Dang
Primary Examiner
Art Unit 2823

4/1/07